10/716,991

cofe



re U.S. Patent No. 6,878,576 B1

EARS ET AL.

Issued: April 12, 2005

For: METHOD FOR MAKING SEMICONDUCTOR)

DEVICE INCLUDING BAND-ENGINEERED SUPERLATTICE Certificate
JUL 2 2 2005
of Correction

REQUEST FOR CERTIFICATE OF CORRECTION OF APPLICANT'S MISTAKE UNDER RULE 1.323

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of Rule 1.323 of the Rules of Practice, the Patent Office is respectfully requested to correct matters in the above-identified patent in accordance with the Certificate of Correction Form PTO-1050 attached hereto.

The Patent Office is requested to issue a Certificate of Correction on the above-referenced Patent Document, and to place such a Certificate of Correction in the file, so that such will appear on any copies of the patent which are ordered in the future.

The corrections being made are of consequence to provide the proper recitation on the cover sheet, in the drawings and specification. Several of the mistakes occurred in good faith and are not the fault of the Patent and Trademark Office. However, one printing error of the Patent Office is also being corrected. No new matter is added by these corrections.

07/18/2005 SFELEKE1 00000036 6878576

01 FC:1811

100.00 OP

In re Patent of MEARS ET AL.
Patent No. 6,878,576 B1
Issued: APRIL 12, 2005

The Commissioner is hereby authorized to charge the requisite fee as set forth in 37 CFR § 1.20(a) in the amount of \$100.00 to the credit card noted in the attached credit card payment form. The Commissioner is authorized to charge or credit any discrepancies in fee amounts to Deposit Account 01-0484.

Respectfully submitted,

CHRISTOPHER F. REGAN

Reg. No. 34,906

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 13th day of July, 2005.

Justin Jan

CERTIFICATE OF CORRECTION

PATENT NO. **DATED**

6,878,576 B1 April 12, 2005

INVENTOR(S)

Mears et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below

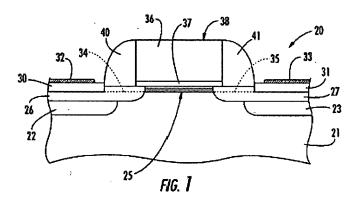
Cover Page, Section

Insert: --H01L 29/14-- after "EP 0393135 11/1994"

56

Cover Page, Drawing

Delete: FIG. 1 Insert: New FIG. 1



MAILING ADDRESS OF SENDER:

PATENT NO. <u>6,878,576 B1</u>

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CERTIFICATE OF CORRECTION

PATENT NO. DATED

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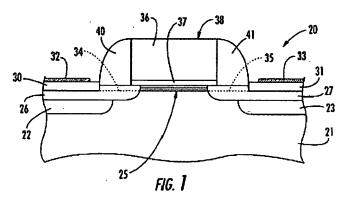
INVENTOR(S)

Mears et al.

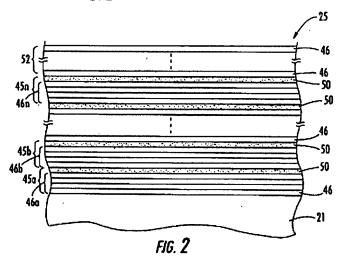
It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below

In the Drawings

Delete: FIG. 1 Insert: New FIG. 1



Delete: FIG. 2 Insert: New FIG. 2



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PATENT NO. ___6,878,576 B1

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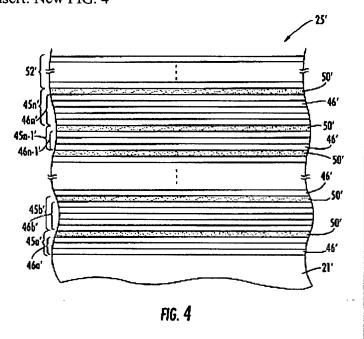
INVENTOR(S)

Mears et al.

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In the Drawings

Delete: FIG. 4
Insert: New FIG. 4



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6,878,576 B1

DATED

April 12, 2005

INVENTOR(S)

Mears et al.

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Column 1, Line 67

Delete: "in a silicon"

Insert: --in silicon--

Column 2, Line 1

Delete: "electromuminescence"

Insert: --electroluminescence--

Column 2, Line 60

Delete: "superlattice and has"

Insert: --superlattice has--

Column 5, Line 14

Delete: "gate 35"

Insert: --gate 38--

Column 5, Line 62

Delete: "gate 35"

Insert: --gate 38--

Column 7, Line 66

Delete: "from the both"

Insert: --from both--

Column 9, Lines

46-48

Delete: "In other processes and devices the structures of

the present invention may be formed on a portion of a

wafer or across substantially all of a wafer."

Column 9, Line 61

Delete: "also formed"

Insert: --also be formed--

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